4.4.3 Selfgating Effect in a Novel Nanometer-Scale Semiconductor Device Utilizing an Asymmetric 2-DEG Channel

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Introduction
We report on a novel III-V semiconductor device utilizing a self-gating mechanism for non-linear carrier transport in a narrow conductive channel. This so-called self-switching device (SSD) was fabricated from an InGaAs/InAlAs/InP semiconductor heterostructure by electron beam lithography and subsequent wet-chemical etching. Current-voltage measurements both at room temperature (RT) and at low temperatures (LT) down to 240 mK reveal a diode-like output characteristic. Exploiting the inherently lateral current control mechanism, the device is extended to field-effect-transistor (FET) by a side gate structure. By using an equivalent circuit model, we are able to describe the basic working principle [1].

For the fabrication of the SSD [2], a MBE-grown high mobility In₀.₅₃Ga₀.₄₇As/In₀.₅₂Al₀.₄₈As/InP two-dimensional electron-gas (2DEG) heterostructure (RT electron concentration: 3.7·10¹² cm⁻², RT mobility 8958 cm²/Vs) is used. The two-dimensional electron-gas system is confined at an In₀.₅₃Ga₀.₄₇As/In₀.₅₂Al₀.₄₈As hetero-interface, only 36 nm below the surface of the sample. The mesa and ohmic contacts are defined by conventional UV photo lithography. Thereafter the geometry of our device is patterned using high-resolution electron beam lithography and subsequent wet-chemical etching.

Fig. 1 Atomic force micrograph of a SSD.
Fig. 2  Output characteristics from the SSD at room temperature.

Figure 1 shows an AFM image of a SSD after processing. The one micron wide channel is narrowed to about 150 nm at the apex of a triangular-shaped constriction. Applying a negative voltage to the upper side of the U-shaped channel, the current inside the narrow region of the channel will be completely pinched-off as a result of the electrostatic field effect from the opposite triangular part of the system. For a positive source-drain voltage the maximum current depends on the channel width at the apex only.

Fig. 3  Output characteristics from the SSD at 240 mK.
Fig. 4 Equivalent circuit model for the SSD.

This device can be further fine-tuned by applying an additional side-gate voltage to the lower contact in order to control the conductance of channel. Using this additional side-gate, the onset source-drain voltage is defined by either the channel geometry or the applied side-gate voltage. Figures 2 and 3 show the output characteristics from our device at room temperature and 240 mK respectively. The traces are recorded at different side-gate voltages. The output characteristics derived from an FET like equivalent circuit model (fig.4) for the SSD are shown in figure 5. Most of the features from our measurements (such as the diode-like characteristic and the shifting onset voltage) are qualitatively well reproduced.

Fig. 5 Simulated output characteristics of the SSD.

References: